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FlowPix: An Image Processing DSL based on an FPGA Overlay Accelerator

Abstract

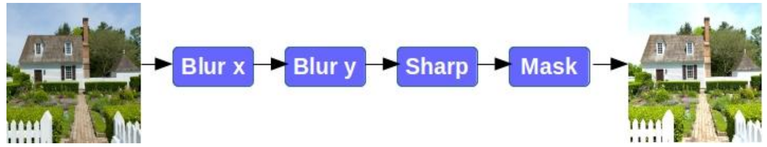


Figure: Unsharp Mask pipeline.

- An image processing pipeline can be viewed as a graph of interconnected stages that processes images successively.
- Image processing algorithms have high spatial and temporal parallelism which makes them favourable for FPGA implementations.
- We propose an overlay based framework to realize image processing algorithms on FPGAs.
- The major goal is to ease programming effort through a DSL, enabling programmers to use FPGAs as target devices.

Hardware Architecture

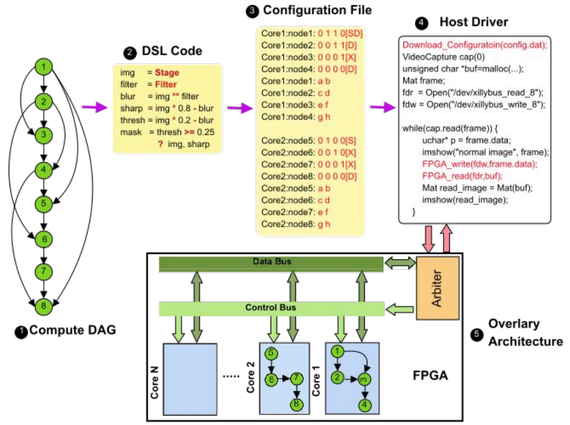
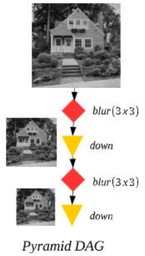


Fig 2. Overall block diagram of our framework.

```
var img = Stage("Path/to/Image")
var down = Filter((2, 2), (2, 2), "max")
var kernel = Filter((3, 3), (1, 1),
                    ((1/16, 1/8, 1/16),
                    (1/8, 1/4, 1/8),
                    (1/16, 1/8, 1/16))
                    )
for(i <- 0 until 2){
 var blur = img ** filter
 var reduce = blur ** down
 img = reduce
}
img.store_image("gaussian_pyramid")
```

Stage	Computation
I	*Input Image*
$blur_0$	$\frac{1}{16}\begin{bmatrix}1&2&1\\2&4&2\\1&2&1\end{bmatrix}$
$down_0$	$\frac{I}{4}$
$blur_1$	$\frac{1}{16}\begin{bmatrix}1&2&1\\2&4&2\\1&2&1\end{bmatrix}$
$down_1$	$\frac{I}{16}$



Pyramid DAG

Fig 3. FlowPix DSL code for a two stage pyramid.

Evaluation

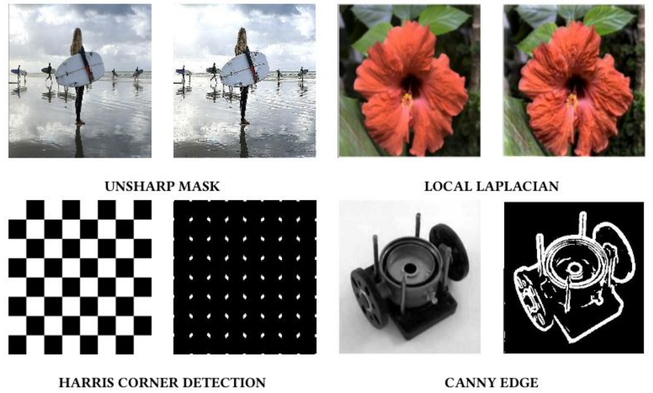


Figure. Few image processing algorithms accelerated by our overlay.

Benchmarks	#cycles	Latency	FPS	PR
Canny Edge	1044484	8.35ms	119	1.003
Harris Corner detection	1040399	8.32ms	120	1.007
Multiscale interpolation	1024143	8.19ms	122	3.94
Unsharp Mask	1044483	8.35ms	119	1.003
Sobel	1044484	8.35ms	119	1.003

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