INTERNATIONAL INSTITUTE OF INFORMATION TECHNOLOGY HYDERABAD

R&D SHOWCASE 2021

Technology, Social Impact

FPGA Accelerator for Stereo Vision using Semi-Global Matching through Dependency Relaxation

ABSTRACT

We propose a fully parallel and pipelined architecture for stereo vision on FPGAs using Semi-Global Matching with Census Transform being used underneath. Further, we extend the above streaming architecture so that multiple pixels can be processed in a data parallel fashion. We expose this data parallelism through dependency relaxation. This establishes a trade-off between accuracy and throughput of the hardware. We tested the proposed architecture on Virtex-7 FPGA using KITTI 2012 and KITTI 2015 datasets. On images of resolution 1280x960, with 64 disparity levels, we are able to run our hardware design at 100 MHz. At this frequency, our design is able to process 322 frames per second which is 1.6 times faster than the state-of-the-art SGM implementation on FPGA.

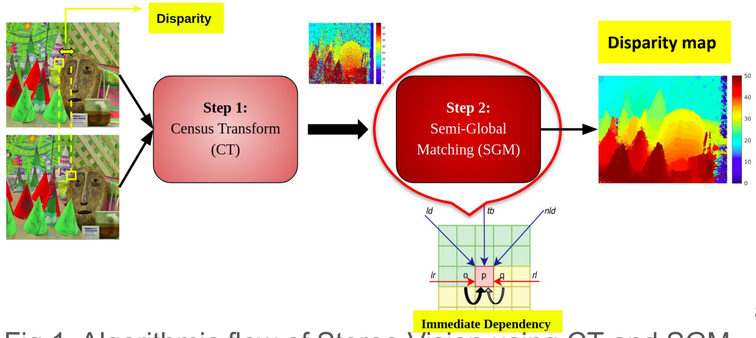


Fig 1. Algorithmic flow of Stereo Vision using CT and SGM.

Hardware Architecture

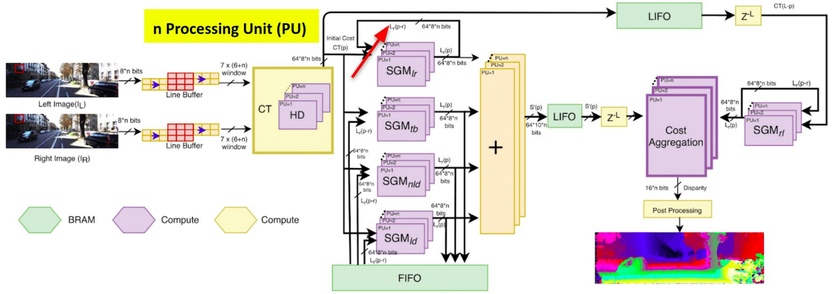


Fig 2. Overall architecture of the proposed stereo vision accelerator with n PUs.

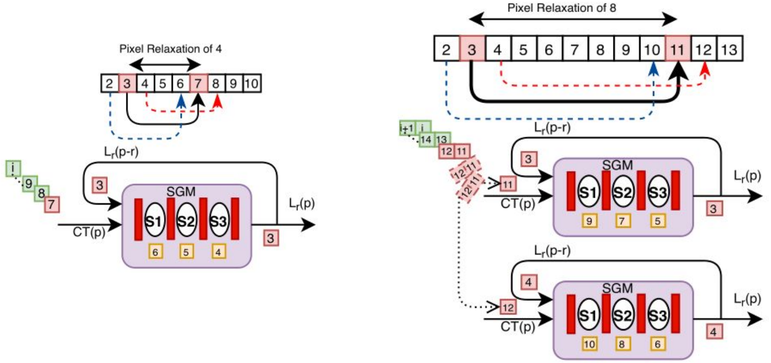


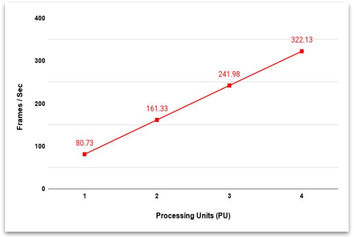
Fig 3. For PU=1 and PU=2, the immediate dependency is relaxed to four and eight, respectively. Dependency relaxation aids the pipeline to function at maximum throughput, and multiple PUs introduce pixel-level parallelism.

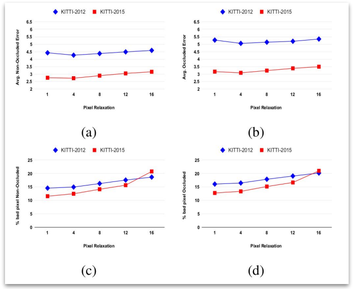
RESULTS

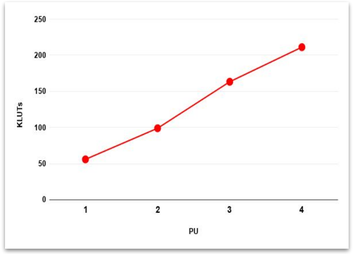
Graph 1: We can achieve an almost linear increase in the processing capability, in terms of Frames Per Seconds (FPS), for every increment in Processing Unit (PU).

Graph 2: The increase in average error was 0.12, and the increase in %-bad-pixel was 1.96% for every increment in PU.

Graph 3: Resource usage in terms of KLUTs was also linear with PUs.







PUBLICATION

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Authors: Shashwat Shrivastava, Ziaul Choudhury, Shashwat Khandelwal, Suresh Purini Computer Systems Group