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Accelerating Local Laplacian Filters on FPGAs

ABSTRACT

Local Laplacian Filtering is an edge-aware image processing technique that can be successfully applied for detail smoothing, detail enhancement, tone mapping and inverse tone mapping of an image. We propose a hardware accelerator, which exploits fully the available parallelism in the algorithm, while minimizing the utilization of on-chip FPGA resources.

Fig 1. Examples of detail and tone manipulation in images.

PROPOSED ARCHITECTURE

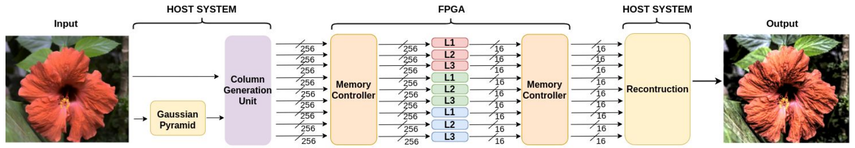

Fig 2. Hardware architecture depicting the flow fo data from the host to the FPGA then back to the host. It shows the example of a detail enhancement operation.

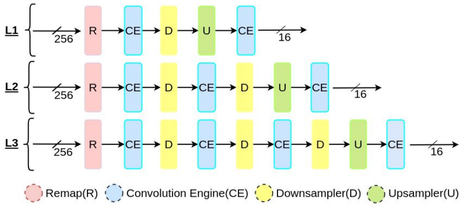

Fig 3. LPU's comprising of a remap unit, convolution engine, a downsampling and an upsampling unit.

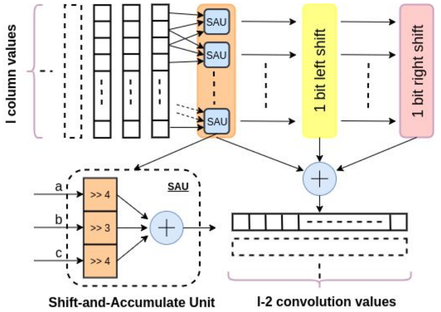

Fig 4. Convolution engine, exploits both pipelined and data parallelism.

RESULTS

On Virtex-7 FPGA, we obtain a 7.5x speed-up to process a 1 MB image when compared to an optimized baseline CPU implementation. This is the first hardware accelerator proposed in the research literature for the Local Laplacian Filtering problem.

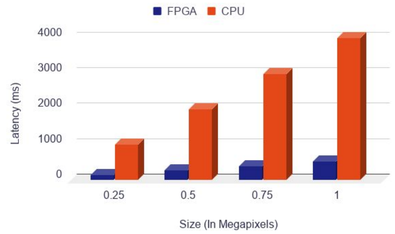

Fig 5. Graph shows the speed up for different sized images.

	β = 1				α = 1		
$\sigma \backslash \alpha$	**0.25**	**0.5**	**2**	$\sigma \backslash \beta$	**0**	**0.5**	**1**
0.1	45.5	48.03	48.33	**0.1**	40.56	45.42	49.98
0.2	40.55	44.88	46.12	**0.2**	43.13	47.37	49.98
0.4	34.75	40.19	40.88	**0.4**	49.94	49.11	49.98

Fig 6. PSNR values comparing the CPU and FPGA implementations for the flower image.

RELATED PUBLICATIONS

Khandelwal, et al. "Accelerating Local Laplacian Filters on FPGAs." *2020 30th International Conference on Field Programmable Logic and Applications (FPL)*. IEEE, 2020.

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